SparsePIM: An Efficient HBM-Based PIM Architecture for Sparse Matrix-Vector Multiplications

Taewoon Kang
Computer Science and Engineering
Korea University
Seoul, Republic of Korea
taewoon_kang@korea.ac.kr

Geonwoo Choi
Computer Science and Engineering
Korea University
Seoul, Republic of Korea
hnts03@korea.ac.kr

Taeweon Suh
Computer Science and Engineering
Korea University
Seoul, Republic of Korea
suhtw@korea.ac.kr

Gunjae Koo
Computer Science and Engineering
Korea University
Seoul, Republic of Korea
gunjaekoo@korea.ac.kr

Abstract

Sparse matrix-vector multiplication (SpMV) is a fundamental operation across diverse domains, including scientific computing, machine learning, and graph processing. However, its irregular memory access patterns necessitate frequent data retrieval from external memory, leading to significant inefficiencies on conventional processors such as CPUs and GPUs. Processing-in-memory (PIM) presents a promising solution to address these performance bottlenecks observed in memory-intensive workloads. However, existing PIM architectures are primarily optimized for dense matrix operations since conventional memory cell structures struggle with the challenges of indirect indexing and unbalanced data distributions inherent in sparse computations.

In order to address these challenges, we propose SparsePIM, a novel PIM architecture designed to accelerate SpMV computations efficiently. SparsePIM introduces a DRAM row-aligned format (DRAF) to optimize memory access patterns. SparsePIM exploits K-means-based column group partitioning to achieve a balanced load distribution across memory banks. Furthermore, SparsePIM includes bank group (BG) accumulators to mitigate the performance burdens of accumulating partial sums in SpMV operations. By aggregating partial results across multiple banks, SparsePIM can significantly improve the throughput of sparse matrix computations. Leveraging a combination of hardware and software optimizations, SparsePIM can achieve significant performance gains over cuSPARSE-based SpMV kernels on the GPU. Our evaluation demonstrates that SparsePIM achieves up to 5.61× speedup over SpMV on GPUs.

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CCS Concepts

• **Computer systems organization** → *Special purpose systems.*

Keywords

Processing-in-Memory, SpMV, Near-Data Processing

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1 Introduction

Sparse matrix-vector multiplication (SpMV) is a fundamental kernel used in a wide range of applications, including scientific computing, machine learning, graph analytics, and circuit simulation [6, 24, 29, 34, 50, 54, 82, 86, 87]. SpMV kernels exhibit extremely low efficiency on general parallel processor architectures and matrix processing engines since those kernels handle large matrices with many zero elements that unnecessarily occupy processing units and storage space. Researchers have proposed specific processor architectures and data compression formats for sparse matrices. However, existing solutions often provoke heavy irregular accesses to the memory hierarchy, thus, the performance of SpMV kernels is significantly restricted by limited memory bandwidth.

Processing-in-memory (PIM) is an emerging approach that can mitigate the performance hurdles caused by constrained memory bandwidth. PIM architectures are implemented by integrating computing units near or within memory cell arrays, thus PIM can exploit high internal bandwidth within a memory package. Moreover, PIM can reduce data movement between processors and off-chip memory modules by offloading computations to memory. Several memory vendors presented PIM solutions, such as HBM-PIM [31, 39, 44]

and GDDR6-AiM [37, 38, 45], demonstrating that PIM solutions are effective for general matrix operations frequently observed in neural network applications. However, the existing PIM solutions cannot handle sparse matrix operations effectively since those solutions rely on regularly structured 2-dimensional memory cell arrays. Note that general representations of sparse matrices include many zero elements, wasting memory space significantly. Furthermore, existing PIM solutions cannot handle compressed sparse matrices efficiently due to the indirect indexing and unbalanced data allocations observed in compressed sparse matrices.

In this paper, we propose SparsePIM, an efficient PIM architecture for accelerating SpMV kernels on 3D-stacked high-bandwidth memory (HBM). SparsePIM features a hardware architecture tailored for SpMV and incorporates software-level optimizations to achieve a significant speedup in SpMV operations on PIM. First, SparsePIM employs a data compression and allocation format aligned with the DRAM row structure to leverage row-buffer locality and reduce the overhead of indirect indexing. SparsePIM also applies K-means-based column grouping to evenly distribute non-zero elements across multiple memory banks and mitigate bank-level load imbalance. Additionally, the software optimization groups matrix columns that include the same row indices, thus SparsePIM can improve computational efficiency by exploiting data parallelism more efficiently. By combining these hardware and software techniques, SparsePIM can significantly improve the performance of SpMV computations on HBM-based PIM.

We evaluate SparsePIM using a modified DRAMSim3 [48] simulator. Our evaluation results exhibit that SparsePIM achieves up to 5.61× speedup compared to SpMV kernels using the cuSPARSE library on a GPU. In addition, the proposed DRAM row-based compression format reduces memory usage by up to 29.82% compared to the conventional coordinate (COO) format. The computation engines in SparsePIM can efficiently parallelize the computations of non-zero elements with the proposed DRAM row-based data allocation format. We also estimate the power and area overhead of SparsePIM. The estimated dynamic power consumption of SparsePIM is 31.85 μW, which meets the thermal design power (TDP) requirements of the existing HBM-PIM.

The following are the contributions of our work.

- We propose SparsePIM, an efficient software/hardware approach for accelerating SpMV computations on HBM-based PIM architecture. SparsePIM's software optimizations and hardware design are specifically tailored to the hierarchical structure of an HBM stack.
- We present efficient software optimization techniques that ensure load balancing in PIM operations and enable effective accumulation of partial results.
- We propose an effective sparse compression format tailored to the memory cell structures of DRAM.
- We propose an efficient and lightweight hardware architecture and instruction set to support SpMV in HBM-based PIM architecture.
- We implement SparsePIM using a cycle-accurate DRAM simulator to evaluate the effectiveness of the proposed software/hardware co-design approach.

2 Background

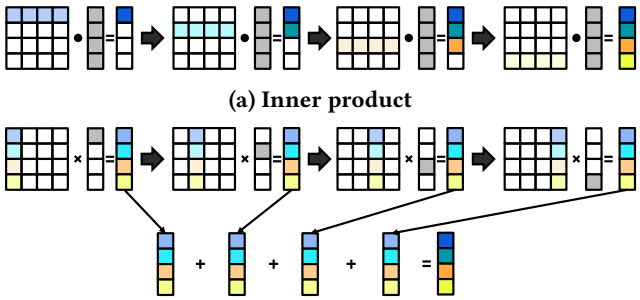
2.1 Sparse compression formats

Although compression formats are widely deployed for reducing the memory footprint of sparse datasets containing a large fraction of zero values, compressed data structures work as critical performance hurdles in parallel architectures. For large-scale applications that rely on SpMV computations, sparse data are represented as large matrices where most elements are zero. Since zero elements waste storage space and computational resources for multiplications, sparse matrices can be efficiently represented by storing only non-zero values and their corresponding indices using compression formats. Modern applications that handle sparse data typically employ compression formats such as coordinate (COO), compressed sparse row (CSR), and compressed sparse column (CSC) formats to represent sparse matrices [71]. Using these compression formats, only non-zero elements are stored along with two-dimensional coordinates in a matrix (i.e., COO) or index pointers to the starting positions of column/row indices (i.e., CSR/CSC formats). Note that processors fetch non-zero elements using the corresponding indices for computing sparse data structures. Hence, computing kernels that handle compressed sparse matrices often create heavy irregular memory accesses to provoke extremely low utilization in processing units and memory systems [36, 90, 91].

In order to handle such performance hurdles by the commonly used sparse data structures, researchers have proposed more efficient compression formats specifically tailored for target processors such as GPUs [4, 14, 51, 60, 79] and domain-specific architectures [47, 52, 53, 68]. Such compression formats can offer more optimized memory access patterns and/or enhanced parallel computations. However, sparse compression formats are not well-explored for PIM architectures that rely on two-dimensional data cell structures.

2.2 SpMV computation methods

SpMV computation can be performed using two different approaches, inner product and outer product, as depicted in Figure 1. The inner product approach performs a conventional dot-product operation between each matrix row and an input vector. By the inner product method, each element



(a) Inner product

(b) Outer product

Figure 1: Comparison of SpMV computation

of a result vector is computed by accumulating partial products computed from elements in a single matrix row and the corresponding elements in an input vector, as shown in Figure 1a. For dense matrix operations, the inner product approach can exploit efficient data-level parallelism in a matrix row and an input vector, and the input vector elements can be reused in local buffers. However, when sparse data structures are involved, the inner product method requires complex index matching with the input vector. Furthermore, since each row of a sparse matrix contains a different number of non-zero elements, the number of multiplications and accumulations varies for each output element. Such irregular processing in SpMV computations can lead to significant performance degradation in regularly organized processing engines [8, 15, 61].

On the other hand, the outer product approach performs a vector-scalar multiplication between a matrix column and a single element of an input vector to compute a partial result vector as depicted in Figure 1b. The partial output vectors computed from the matrix columns are accumulated to generate the final result vector. For SpMV operations, the outer product approach can perform multiplications between non-zero elements in a matrix column and a single element in an input vector to generate partial results associated with the row indices of the corresponding non-zero elements. Then, the partial results associated with the same row indices are accumulated to generate the element in the final result vector. Unlike the inner product approach, which requires index matching between non-zero elements in a row and an input vector, the outer product approach performs simple element-wise multiplications between a non-zero vector and a scalar. The generated partial results associated with row indices can be accumulated immediately once generated. However, the outer product approach requires additional memory space for storing the intermediate partial results. Thus, efficient dataflows and buffer management mechanisms are essential to mitigate the storage overhead of the outer product method [25, 65].

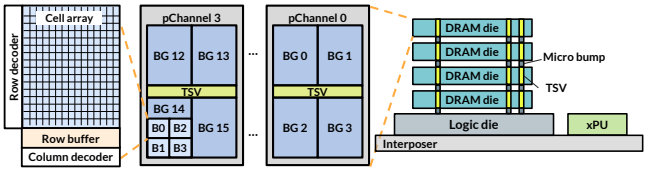


Figure 2: HBM architecture and organization

2.3 High bandwidth memory

High bandwidth memory (HBM) is an advanced memory technology that employs 3D-stacked memory dies mounted on a silicon interposer and vertically connected data channels to provide higher data bandwidth and energy efficiency compared to traditional DRAM [7, 9, 23, 40–43, 56, 57, 63, 67, 76]. As illustrated on the right side of Figure 2, the multiple memory dies in HBM are interconnected using through-silicon vias (TSVs), which allow high-speed data communication between layers [23, 32]. In HBM, multiple memory dies are stacked on a logic die (also called a base die) that includes peripheral circuits such as I/O drivers, data buffers, and a physical interface (PHY). The logic die interfaces with processors (xPU in the figure) through the silicon interposer by managing data transfers from the stacked memory dies. A memory die includes DRAM cells that store data. Each memory die works like a traditional DRAM chip.

The left side of Figure 2 depicts the hierarchical structure of HBM. A single HBM stack includes multiple channels, and each channel supports 128-bit wide data transfers. Each channel is logically divided into two 64-bit pseudo-channels (denoted as pChannel in the figure) to increase parallelism in memory operations. The two pseudo-channels within a physical channel have separate command and address buses but share the same 128-bit data channel. Each pseudo-channel covers several bank groups (BG in the figure), and each bank group includes multiple banks (B in the figure).

A bank is a basic data cell unit that operates independently by memory read and write commands. Each bank includes data cells organized into multiple rows as shown in Figure 2. During a read operation, a specific row is activated using a row address, and then the data in the activated row is loaded into the row buffer (i.e., sense amplifiers) via bit lines. The data in the row buffer is further multiplexed by a column address, then the selected column data is read out. Namely, a row represents the basic access granularity within a bank. In HBM2, the size of a single row is 1 KB [57].

2.4 HBM-based PIM

Processing-in-memory (PIM) is an architectural idea that integrates computation capabilities into memory components to reduce the performance overhead caused by data

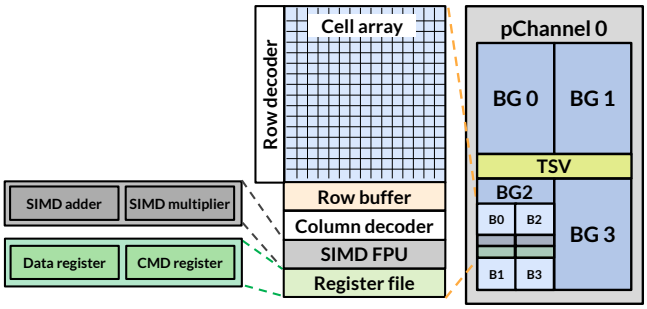


Figure 3: HBM-PIM architecture

transfers from external memory. Recently, a memory vendor demonstrated an HBM-based PIM solution, called HBM-PIM [31, 39, 44]. In order to implement a PIM-enabled die, HBM-PIM integrates SIMD-like processing units and register files into a memory die as shown in Figure 3. Note that these processing elements occupy the die area, thus, half of the rows in a DRAM bank are replaced with the logic elements on a PIM die.

HBM-PIM supports two distinct operation modes, a single-bank (SB) mode and an all-bank (AB) mode. In SB mode, HBM-PIM behaves like conventional memory devices, namely, memory commands are issued to only a single target bank specified by a bank address. In contrast, AB mode is designed to facilitate PIM operations in HBM-PIM to exploit parallel operations by activating multiple banks. In AB mode, a bank address is ignored, thus, memory commands are broadcast to all banks simultaneously. To initiate PIM operations of HBM-PIM, a host processor transfers a special command sequence to change the operation mode of HBM-PIM to AB mode. Then, the PIM dies in HBM-PIM can concurrently execute PIM instructions triggered by column commands.

HBM-PIM supports several RISC-type instructions to perform PIM operations. The instruction set of HBM-PIM includes control, arithmetic, and data movement instructions [44]. Since HBM-PIM is primarily designed to support general matrix-vector operations, HBM-PIM does not include instructions that can support indirect indexing, which is observed frequently in sparse data processing.

3 Related work

SpMV on PIM: SpMV operations are memory-intensive kernels since SpMV can create many irregular memory transactions from its indirect indexing mechanisms. Several researchers have explored PIM-based solutions that can accelerate SpMV computations by leveraging high internal bandwidth and parallel computation capabilities of PIM architectures.

SpaceA is a PIM solution for accelerating SpMV operations on hybrid memory cube (HMC) [88]. SpaceA employs two-level content-addressable memories (CAMs) to perform cache tag matching more efficiently in processing engines. SpaceA also utilizes software optimizations to distribute non-zero elements evenly across multiple memory banks. SpaceA assigned the row data of sparse matrices to rows in a bank to optimize row data accesses. SpaceA exploits a unique feature of HMC that allows internal data movement across memory dies. However, currently, HMC is not a standardized memory device, thus, the impacts of SpaceA may be limited.

pSyncPIM is an HBM-based approach that can accelerate SpMV and sparse triangular solve (SpTRSV) operations [5]. pSyncPIM proposes a partial synchronous execution mode that can accommodate irregular accesses and computations more efficiently. pSyncPIM employs semi-independent bank operations to minimize idle times of PIM operations. pSyncPIM tackles the synchronous executions in HBM-PIM, however, pSyncPIM does not address the inefficient indexing caused by conventional compression formats.

SpDRAM [27] is a DRAM-based SpMV acceleration approach that exploits bit-serial operations [74]. SpDRAM leverages in-DRAM bitwise computations to perform arithmetic operations. SpDRAM presents a data allocation method that can support bit-serial operations efficiently. However, SpDRAM requires complex bit-level control mechanisms to fully exploit the bit-serial operations.

PIM architectures: PIM is an emerging research area actively explored by both industry and academia. Major memory vendors have demonstrated their PIM solutions based on existing memory technology. Samsung presented HBM-based PIM solutions [31, 39, 44]. AiM is a PIM architecture implemented on GDDR6 [16, 37, 38, 45]. UPMEM is a commercialized PIM solution based on DRAM [10, 64]. Academic researchers have also presented PIM architectures based on 3D-stacked memory technology [1–3, 11, 21, 25, 58, 69, 81, 89, 92–96]. PIM solutions have been further investigated for modern large-scale AI systems [18, 64, 73].

SpMV computations: As SpMV is a core compute kernel for a wide range of applications, researchers have presented efficient hardware/software solutions for SpMV. In order to exploit data locality in SpMV kernels, researchers have proposed software optimizations such as tiling [8, 12, 15, 46, 59, 61] and reordering [12]. Several researchers have worked on hardware accelerator architectures that can handle irregular computations and memory accesses in SpMV kernels more efficiently [13, 19, 19, 28, 33, 47, 49, 53, 65, 68, 72, 77, 78, 83].

4 Motivation

The performance overhead of SpMV kernels becomes more critical as modern applications employ large-scale sparse data structures. In order to handle the storage overhead of numerous zero elements, SpMV kernels typically employ

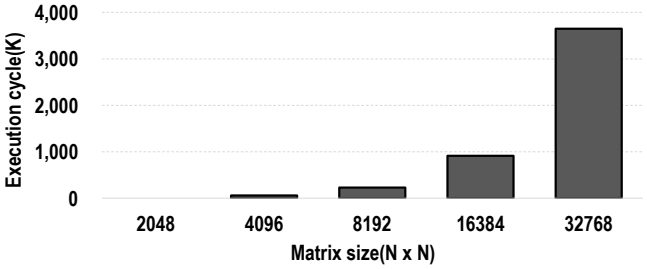


Figure 4: Execution cycle of SpMV on HBM-PIM by the size of a sparse matrix

sparse compression formats. However, as described in Section 2.1, compressed sparse data structures include index information along with non-zero elements (NZEs), thus, the indirect indexing in compressed sparse matrices causes significant inefficiency in both processing units and memory systems [26, 35]. Furthermore, non-zero elements are not uniformly distributed across columns/rows in a sparse matrix, leading to significant load imbalance in computations in columns/rows. For example, graph data structures used in graph analytics and neural network applications often follow power-law distributions in the number of non-zero elements per row or column. Note that the overall performance of SpMV kernels is usually determined by the row/column that includes a large number of non-zero elements. As a result, such applications experience serious performance degradation when processing rows or columns in parallel [22, 30]

In particular, the performance issues caused by load imbalance in SpMV should be addressed seriously when SpMV kernels are executed on PIM-based architectures since the processing units in PIM architectures are tightly coupled with banks or bank groups in a memory package. Note that the row/column data in a large sparse matrix are allocated across multiple banks (or bank groups) in a memory package and data communications across banks (or bank groups) are typically restricted. Hence, if non-zero elements are non-uniformly allocated in multiple banks, it causes significant performance drops due to imbalanced computations among bank-level processing engines. In order to mitigate such issues, software-based optimizations are required to balance the distribution of non-zero elements across banks (or bank groups) associated with the processing units.

To accommodate SpMV computations efficiently on PIM platforms, the hardware architectures in PIM or logic dies are specifically designed to support sparse data structures. However, commodity PIM solutions such as HBM-PIM and GDDR6-AiM are primarily tailored for general matrix-vector operations. In order to investigate the performance burdens by large-scale sparse matrix operations, as shown in Figure 4 we measure the performance of SpMV formatted in a general matrix structure using a DRAMsim3-based HBM-PIM simulator [48]. Our experiment results exhibit that the execution cycles of the SpMV kernel increase exponentially as the matrix size grows. Our analysis reveals that the current HBM-PIM architecture is significantly inefficient for computing large-scale sparse matrices.

5 SparsePIM

In this paper, we propose *SparsePIM*, an efficient PIM architecture optimized for SpMV computations. As discussed in the previous section, PIM solutions require software-based optimizations and specific hardware architectures to tackle the performance overhead of large-scale SpMV kernels. SparsePIM employs software approaches that can distribute non-zero elements evenly across multiple banks and bank groups. For this purpose, SparsePIM utilizes a K-means-based simple partitioning algorithm. We also propose a new sparse data compression format, called a DRAM row-aligned format (DRAF), tailored to the data cell structures of DRAM. Our proposed compression format minimizes data movement between DRAM data cells and processing engines to improve processing efficiency for generating partial results of outer product computation for SpMV. Moreover, SparsePIM incorporates partial result accumulators associated with bank groups to reduce the number of partial products quickly. By combining both software and hardware approaches, SparsePIM can perform large-scale SpMV computations efficiently within an HBM stack.

SparsePIM performs SpMV operations using an outer product approach, as described in Section 2.2. The outer product-based SpMV computations by SparsePIM are executed hierarchically based on the hierarchical structures in an HBM stack (see Section 2.3. A SIMD floating-point unit (FPU) associated with two neighboring banks (i.e., even/odd banks within a bank group) computes vector-scalar multiplications using non-zero elements in a matrix column and a single element from an input vector. The corresponding bank group includes a bank group accumulator (BGA) that accumulates partial results generated from the banks within the bank group.

5.1 Software optimizations

SparsePIM performs vector-scalar multiplications for the outer product operation of SpMV using processing engines in multiple banks. Hence, as described in Section 4, non-zero elements in a sparse matrix should be loaded evenly across banks. Furthermore, SparsePIM's efficiency can be improved if non-zero elements associated with the same row indices are grouped within a single bank group. Note that SparsePIM performs accumulations of partial results using bank group

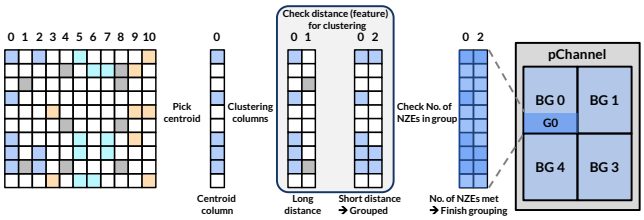


Figure 5: Simplified execution flow of grouping columns based on row index similarity.

accumulators. Consequently, SparsePIM employs software-based optimizations to achieve higher computational efficiency.

Figure 5 depicts how SparsePIM's software-based optimization clusters the columns of a sparse matrix. In this example, we assume the size of the sparse matrix is 10×10 and the colored blocks represent non-zero elements (NZEs) in the matrix. First, SparsePIM selects a reference column randomly as a centroid column (*column 0* in the figure). Then, SparsePIM computes the *row-index similarity* (i.e., the number of NZEs that share the same row indices with NZEs in the reference column) of a different column based on the centroid column. In this example, *column 1* and *column 2* have row-index similarities of 1 and 3, respectively, when compared to *column 0*. As a result, *column 2* is grouped with the centroid column (i.e. *column 0*) and assigned to the same bank group. Note that the grouped columns include more NZEs that share the same row indices, thus, more partial results generated by the outer product operation can be efficiently accumulated by a bank group accumulator (BGA).

We choose K-means as the base clustering algorithm for sparse matrices [75]. K-means clustering exhibits low computation cost compared to other clustering algorithms [20, 70, 85]. Since SparsePIM incorporates a fixed number of bank groups associated with processing units, we set the number of clusters equivalent to the number of PIM bank groups when K-means clustering is applied. However, simple K-means clustering cannot guarantee an even distribution of non-zero elements across bank groups. In order to address this issue, SparsePIM employs a modified clustering algorithm, referred to as *bounded cap K-means*, and an additional *refinement* step for balancing the distribution of non-zero elements further.

SparsePIM's software optimization algorithm is described in Algorithm 1. The algorithm receives the data structures, *nNZE(c)* and *fmap(c)*, of each column in the sparse matrix. *nNZE(c)* denotes the number of non-zero elements (NZEs) in the column *c*, and *fmap(c)* is a feature map that represents the mapping information of non-zero elements. The behavior of the algorithm is controlled using the hyperparameters.

Algorithm 1 Software optimizations based on K-means

Input: col.nz[] (each c has nNZE(c), fmap(c)), k, maxIter, refineIter, delta, th
Output: col.bg[] (where col.bg[c] = assigned bg index (0...k-1))

$totalN = \sum_c nNZE(c)$
$minCap = (totalN/k) \cdot (1 - delta)$
$maxCap = (totalN/k) \cdot (1 + delta)$

Bounded cap K-means (iteration no. = maxIter):
Initialize centroids[] ← random columns
for each column **c** in col.nz[] **do**
  for each **bgIdx** = $0 \ldots k-1$ **do**
    if $nNZE(col.bg[\textbf{bgIdx}]) + nNZE(c) \leq maxCap$ **then**
      $cost \leftarrow distance(fmap(c),\ centroids[\textbf{bgIdx}])$
      if $nNZE(bg) < minCap$ **then**
        $cost \leftarrow 0.5 \times cost$ (discount cost)
      end if
    end if
    assign **c** to the col.bg[**bgIdx**] with the smallest cost
  end for
  if no suitable cluster found **then**
    assign *c* to the smallest $nNZE(col.bg[\textbf{bgIdx}])$
  end if
end for
Update centroids (avg. each cluster's fmap(c))

Refinement (iteration no. = refineIter):
Identify **"big cluster"** and **"small cluster"** in col.bg[]
for each column **c** **do**
  if moving **c** from **big cluster** to **small cluster and** distance change < th **then**
    Move **c** to **small cluster**
  end if
end for
if no improvement **then**
  break
end if

return col.bg[]

k specifies the number of partitions, corresponding to the total number of bank groups for PIM operations in the HBM stack. *delta* adjusts the min/max boundary condition (i.e., *minCap* and *maxCap*) of the number of NZEs in each cluster. Namely, *delta* adjusts the deviations from the average number of NZEs in each cluster. Note that all clusters should contain the same number of NZEs to ensure balanced PIM operations across clusters (i.e., bank groups). However, enforcing this constraint may reduce the row-index similarity

within a cluster. SparsePIM utilizes *delta* to trade off the load balancing of PIM operations and row-index similarity. *th* sets the distance threshold for balancing the distribution of NZEs across clusters. Finally, *maxIter* and *refineIter* define the number of iterations for the *bounded cap K-means* and *refinement* steps, respectively.

Bounded cap K-means: SparsePIM exploits a K-means clustering algorithm to group sparse matrix columns that share the same row index values. Note that a traditional K-means algorithm clusters elements based on Euclidean distance between elements. SparsePIM's *bounded cap K-means* algorithm computes the Euclidean distance between columns using the feature maps (i.e., *fmap*), which represent the row indices of NZEs in the column. The clustering process begins by randomly selecting a centroid column for each cluster. Similar to traditional K-means, SparsePIM iteratively updates the centroid of each cluster based on the computed Euclidean distances from the centroid. SparsePIM uses the row-index similarity calculated using the feature maps of the sparse matrix columns as *distances*. However, traditional K-means cannot guarantee the even distribution of non-zero elements across clusters since each column includes a divergent number of non-zero elements, and the algorithm only considers the distances between feature maps. Hence, SparsePIM sets the constraints (i.e., *minCap* and *maxCap*) that define the allowable range of NZEs per cluster. The bounded-cap K-means process terminates either when the maximum number of iterations is reached or when the centroids no longer change.

Refinement: SparsePIM further leverages the refinement process to guarantee load balancing in PIM operations per bank group. Since the K-means-based clustering algorithm primarily considers the row-index similarity from the centroids, the clusters may exhibit significant variation in the number of NZEs. SparsePIM applies the refinement step to reduce imbalances in NZE distribution among bank groups. In each iteration, SparsePIM picks a *big cluster* (i.e., the cluster containing NZEs more than the average) and a *small cluster* (i.e., the cluster containing fewer NZEs). SparsePIM tries to move an arbitrary column from the *big cluster* to the *small cluster* and evaluate the distance change. If the distance change is less than the threshold (*th*), SparsePIM allows the move of the selected column. The refinement process continues until the maximum number of iterations (*refineIter*) is reached, or no further improvements can be made.

One of the main reasons SparsePIM employs a K-means-based clustering approach is its relatively fast execution time compared to other methods. In order to evaluate this advantage, we compare our proposed software optimization methodology with the preprocessing technique presented in SpaceA [88]. Whereas SparsePIM performs the column-based grouping, SpaceA clusters rows of a sparse matrix.

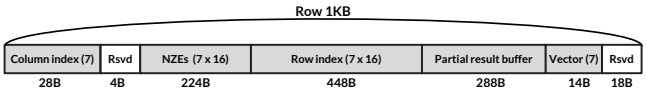


Figure 6: DRAM row-aligned format for a DRAM row

SpaceA proposes a preprocessing strategy that improves computational efficiency through data reuse by organizing partitioned rows such that their internal non-zero elements share similar column indices. This preprocessing consists of two stages: *assignment of rows to logical PEs* and *assignment of logical PEs to physical PEs*. Among these, the first stage dominates the overall execution time, resulting in a time complexity of $O(N_{PE} \times N_{NZE} \times \log N_{NZE})$.

In contrast, SparsePIM's optimization technique assigns columns to clusters during the *bounded cap K-means* process by comparing all data points (n) based on the total average number of non-zero elements (same as N_{NZE}), (d) based on the average number of non-zero elements per column, and iterating over the k clusters. This results in a time complexity of $O(nkd)$. Since the clustering process is repeated for t iterations, the overall complexity becomes $O(nkdt)$. For the *refinement* process, all clusters are evaluated to identify a *big cluster* and a *small cluster*, and the columns within the selected *big cluster* are traversed to determine whether they should be reassigned. Repeating this process for *refineIter* iterations (r) yields a complexity of $O\left(k \times \frac{n}{k} \times r\right) = O(nr)$. Since both the K-means iterations (t) and the refinement iterations (r) are much smaller than n (i.e., $t, r \ll n$), the final time complexity is dominated by $O(nkd)$. In conclusion, the time complexities of the preprocessing strategies in SpaceA and SparsePIM depend on the relative magnitudes of d and $\log(N_{NZE})$, and may vary depending on the distribution of non-zero elements in the matrix. As a result, the two approaches exhibit different performance characteristics across varying sparsity patterns.

5.2 DRAM row-aligned format

SparsePIM employs a column-oriented sparse compression format designed to align with DRAM's row structure. Note that the existing sparse compression formats include index information that represents the positions of non-zero elements in a sparse matrix. However, such indexing mechanisms require indirect accesses, which are significantly inefficient for DRAM's two-dimensional data cell structures. In order to address such issues, SparsePIM adopts the outer product approach for SpMV and an efficient compression format aligned with DRAM rows. We call this sparse compression format DRAF (DRAM row-aligned format).

Figure 6 exhibits the data organization formatted by DRAF. In each data field, the number in brackets indicates the number of elements. We assume that the size of a single element in matrices and vectors is 2 bytes (i.e., FP16 precision) and a single column/row index occupies 4 bytes. Since SparsePIM implements its PIM architecture on HBM2, we assume that DRAF is applied based on 1 KB of DRAM row size [57]. Based on DRAF, SparsePIM assigns necessary operands and indices within the data field of a single DRAM row as shown in the figure. Note that SparsePIM performs an outer product operation between non-zero elements (NZEs) in a matrix column and a single element in a vector (see Section 2.2). In order to support the outer product operations using the data in a row buffer, SparsePIM encapsulates a column index, NZEs, and the corresponding row indices from a matrix column. Under the HBM2 configuration, SparsePIM can store up to seven matrix columns within a single DRAM row, and each column can contain a maximum of 16 NZEs. If a single matrix column includes more than 16 NZEs, the remaining NZEs are assigned to a new column data group that retains the same column index. Following the DRAF structure, SparsePIM also allocates a data field for storing the computed partial results (i.e., partial result buffer in Figure 6). Unlike the prior outer product-based SpMV accelerators, SparsePIM utilizes the DRAM row buffer to store the partial results, thus, SparsePIM does not require additional storage space. Note that DRAF already includes the row indices field, thus, SparsePIM does not store row indices associated with the partial results. The partial result field can also hold up to 112 partial results. The scalar elements from the input vector are stored in the vector field. Since a single DRAM row includes seven columns in the matrix, SparsePIM also stores the corresponding seven vector elements with DRAF. DRAF includes reserved fields (marked as Rsvd) to align with the 32-byte DRAM column access granularity.

5.3 Hardware architecture

In order to support the vector-scalar multiplications and the accumulations of partial results, SparsePIM incorporates processing units such as SIMD FPU and bank group accumulators (BGAs). The left side of Figure 7 describes the hardware components added to a bank group in an HBM stack. As explained in Section 2.3, a single bank group of HBM2 consists of four banks. Similar to prior HBM-PIM, SparsePIM relies on a register file and a 16-lane SIMD FPU that supports FP16 multiplications and additions associated with a bank [31, 39, 44]. Note that the number of lanes in the SIMD FPU is designed to align with the 32-byte DRAM column access granularity. As shown in the figure, a single SIMD FPU is shared by two banks (i.e., even and odd banks). SparsePIM stores the PIM instructions generated from a microkernel in

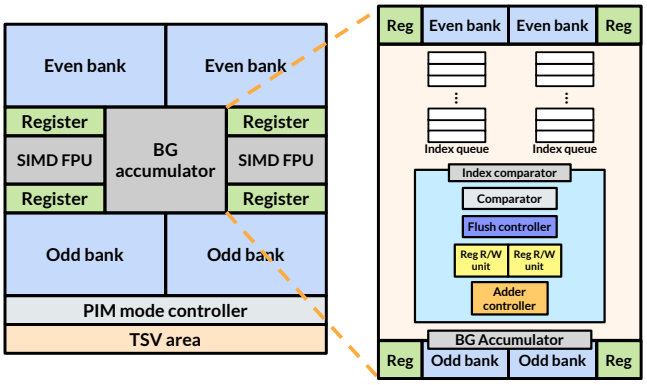


Figure 7: Hardware architecture of processing units in a bank group

Table 1: PIM instructions added in SparsePIM

(a) SparsePIM instructions

Operation	Source A	Source B	Destination
BACC	Row buffer	Data register	BGA
BMOV	Row buffer	-	Scalar register

(b) Instruction format

	31	30	29	28	27	26	25	24	23	22	21	...	8	7	6	5	4	3	2	1	0
BACC	OPCODE				Unused			SRC0			Unused			SRC0 Idx				Unused			
BMOV	OPCODE				Unused																

command registers, and these instructions are triggered by memory commands like HBM-PIM. As a result, SparsePIM can operate using conventional DRAM command sequences.

5.3.1 SparsePIM instructions.

SparsePIM adds two PIM instructions, *BMOV* and *BACC*, to the base instruction set of HBM-PIM [44]. Table 1 presents the instruction formats and target components of the newly added instructions. *BMOV* moves the selected element from the *vector* field of the row buffer data (see Figure 6) into the scalar register. Note that SparsePIM performs vector-scalar multiplications for outer product operations using a column of a matrix and an input vector element. *BMOV* reads the target vector element selected by *SRC0Idx* from the row buffer and stores the read element in the scalar register. *BACC* is used for accumulating partial results with the bank group accumulator (BGA). When *BACC* is executed, SparsePIM reads eight index values from the *row indices* field in the row buffer, then transfers the index values to the row index queue in BGA. *BACC* selects the target index data using *SRC0Idx*. The corresponding partial results in the data register are also transferred to the index queue simultaneously. Once the index queue is filled, BGA can initiate the accumulation process.

5.3.2 Bank group accumulator (BGA).

The right side of Figure 7 depicts the architecture of a BGA. SparsePIM exploits BGAs to accumulate the partial results associated with the same row index, thus, SparsePIM can reduce the number of partial results effectively. Since all banks within the same bank group share a single BGA, the partial results computed by these banks are aggregated in the BGA. Note that SparsePIM relies on software optimizations to allocate columns with high row-index similarity to the same group, as described in Section 5.1. Hence, the BGA within a bank group can find the partial products associated with the same row index with a higher probability.

A BGA incorporates two index queues where each entry contains a partial result along with the corresponding row index. When SparsePIM executes the *BACC* instruction, the row index values in the *row indices* field in a row buffer and the partial results in the data registers are transferred to the entries in the index queue. Note that the size of a single DRAM column is 32 bytes, thus, SparsePIM fills eight entries per *BACC* instruction. In this paper, we set the depth of each index queue to 16, considering the power constraint of an HBM stack.

The BGA performs the accumulation process using an index comparator unit composed of a comparator, a flush controller, register read/write units, and an adder controller. In order to accumulate partial results within a bank group, the BGA matches row index values one by one from the index queues and executes the corresponding accumulation operations [17, 55, 72, 84]. The index comparator inspects the head entries of the index queues to compare the row index values. If the index values match, BGA accumulates the partial results associated with the row index. Then, the accumulated result is assigned to one of the register read/write units, and zero is allocated to another register read/write unit. The register read/write units write the accumulated result and zero back to the target data registers, thus one of the data registers can contain the merged partial result. If the index values in the head entries are not equivalent, BGA dequeues the head entry that has a smaller index value. Note that row indices are pre-sorted by SparsePIM's software optimization while the elements of a sparse matrix are compressed and encapsulated using the DRAM row-aligned format (DRAF). This accumulation process is repeated until the index queues are empty.

To prevent overflows of the index queues, the BGA includes a flush controller that can clear the index queues. Since the accumulation process of BGA performs the index matching one-by-one, consecutive *BACC* instructions may cause the index queues to overflow. To address this, the BGA flushes the index queues if one of the index queues includes more than nine valid entries and a *BACC* instruction is executed. This flushing mechanism is required to maintain the sorted order of row indices within the index queues. The adder controller in the BGA is designed to utilize the SIMD adder in HBM-PIM more efficiently. The adder controller transfers operands from the register read/write units to the FP adders. Note that the SpMV microkernel of SparsePIM uses only the SIMD multiplier for vector-scalar multiplications of the outer product approach, thus, the SIMD adder remains idle. The adder controller utilizes this idle resource by allocating partial results to the SIMD adder when the *BACC* instruction is executed.

5.4 Execution flow

We now describe the overall execution flow of SparsePIM. Initially, HBM is set to single-bank (SB) mode to operate the HBM stack as a standard memory device. SparsePIM performs the software optimizations to partition the columns of a sparse matrix and balance the number of non-zero elements across the bank groups in the target HBM stack. SparsePIM compresses the sparse matrix and the input vector using the DRAM row-aligned format (DRAF) as described in Section 6.5. Then, SparsePIM stores the formatted data to the target bank groups on PIM dies of the HBM stack.

In order to enable the PIM operations of HBM-PIM, SparsePIM switches the operation mode to all-bank (AB) mode. Then, SparsePIM programs the compiled PIM instructions for SpMV operations to the command registers in the bank groups. SparsePIM initiates the execution of the PIM instructions by issuing DRAM commands for PIM operations. Since the HBM stack is set to AB mode, all PIM operations of the bank groups on PIM dies are synchronized.

SparsePIM performs the vector-scalar multiplications of the outer product SpMV computation as follows. Using the *BMOV* instructions, SparsePIM reads one of the vector elements in the *vector* field in the row buffer of the bank and stores it in the scalar register. Then, SparsePIM performs vector-scalar multiplications with the SIMD multipliers using the 16 non-zero elements from the *NZEs* field in the row buffer and the vector element in the scalar register. The 16 partial results are stored in the data register.

Next, SparsePIM performs the partial result accumulations using the bank group accumulator (BGA). SparsePIM initiates the accumulation process using the *BACC* instruction. Then, the row index values in the *row index* field in a row buffer are transferred to the index queues in the BGA. Since the size of a single index value is 4 bytes, SparsePIM issues two DRAM column commands to load 64 bytes of the row index data. The BGA operates in a pipelining manner as explained in the previous section. The accumulated partial results are then written back to the data register.

SparsePIM repeats the vector-scalar multiplication and accumulation process seven times since a DRAF encapsulates seven columns of the sparse matrix. Finally, the accumulated

Table 2: Configurations of SparsePIM and baseline

Component	Configuration
SparsePIM	
Memory type	HBM2
No. of pChannels	16
No. of BG / pChannel	4
No. of banks / BG	4
No. of DRAM rows	16,384
No. of DRAM columns	64
No. of SIMD FPU / BG	2
No. of BGA / BG	1
Clock frequency	1 GHz
Timing parameters	$t_{CCDS} = 1$, $t_{CCDL} = 2$, $t_{RAS} = 34$, $t_{RP} = 14$, $t_{RCDRD/WR} = 14$, $t_{RRDS} = 4$, $t_{RRDL} = 6$
Baseline (NVIDIA RTX3090)	
No. of CUDA cores	10,496
Clock frequency	1,395 MHz / 1,695 MHz
Memory bandwidth	935.8 GB/s
Device memory	24 GB GDDR6X

Table 3: Workload

Workload	Domain	Size	Ratio of NZEs
(w1) cant	SE	62,451	5.218E-04
(w2) crankseg_2	SE	63,838	1.744E-03
(w3) lhr71	Chem	70,304	3.092E-04
(w4) pdb1HYS	CB	36,417	1.652E-03
(w5) rma10	CFD	46,835	1.082E-03
(w6) soc-sign-epinions	SNA	131,828	4.841E-05
(w7) Stanford	WGA	281,903	2.910E-05
(w8) bcsstk32	SE	44,609	5.174E-04
(w9) consph	SE	83,334	4.387E-04
(w10) ct20stif	SE	52,329	5.023E-04
(w11) ohne2	SDS	181,343	3.364E-04
(w12) pwtk	SE	217,918	1.248E-04
(w13) shipsec1	SE	140,874	2.004E-04
(w14) ASIC_100k	CS	99,340	9.669E-05
(w15) xenon2	MS	157,464	1.559E-04
(w16) webbase-1M	WGA	1,000,005	3.106E-06

partial results are stored in the *partial result buffer* field in the row buffer using the *MOV* instruction.

6 Evaluation

6.1 Methodology

For performance evaluation, we employ a cycle-accurate simulator modified from DRAMSim3 [48]. Detailed system parameters are summarized in Table 2. In order to align with the thermal design power (TDP) and logic area assumptions of prior work [31, 39, 44], processing logic is placed on only four DRAM dies, while the remaining four dies contain no logic circuits. The simulator is configured to accurately measure the number of execution cycles consumed by both memory transactions and computation.

To evaluate SpMV performance, we implement a micro-kernel in assembly based on the custom instruction set described in Section 5.3.1. The kernel is loaded through memory write commands into the command register, enabling the simulator to model realistic instruction execution. Since each vector-scalar multiplication produces 16 partial results per one *MUL* command, the kernel is written to issue two consecutive *BACC* instructions, each processing eight row indices from the DRAM row buffer.

For comparison, we also evaluate SpMV execution on an NVIDIA RTX3090 GPU using cuSPARSE [62] as the baseline. The RTX3090, based on the Ampere architecture, is used to ensure architectural consistency with the RTX3080 evaluated in pSyncPIM [5]. RTX3090's specifications are also included in Table 2. GPU performance is measured using *cudaEvent*, recording the elapsed time from host-to-device data transfer to host-side retrieval of computation results. The reported execution time is the average of five independent runs conducted on a real system to account for execution time variability inherent in real-world environments. For SparsePIM, we measure the time from kernel programming into the command register and initialization to computation completion and result retrieval.

For power and area analysis, we synthesize the SystemVerilog code using Synopsys Design Compiler. Given that DRAM manufacturing nodes such as 1ynm, 1znm, and 1anm are fabricated using sub-14nm technology [66, 80], we adopt the SAED 14nm FinFET process to evaluate the hardware characteristics of our design.

6.2 Workload

The sparse matrix suite used for evaluation is summarized in Table 3. Each matrix is categorized by its application domain, number of dimensions, and the Ratio of non-zero elements (Ratio of NZEs), which is computed as the ratio of the number of non-zero elements to the total number of matrix elements. For compact representation, domain names are abbreviated as follows: SE denotes structural engineering, Chem refers to chemical process simulation, WGA corresponds to web graph analysis, CB to computational biology, SNA to social network analysis, CFD to computational fluid dynamics, SDS to semiconductor device simulation, CS to circuit simulation, and MS to material science. Using this benchmark suite, we evaluate the performance of the proposed architecture, highlighting the benefits of applying software optimization and employing the DRAF compression format.

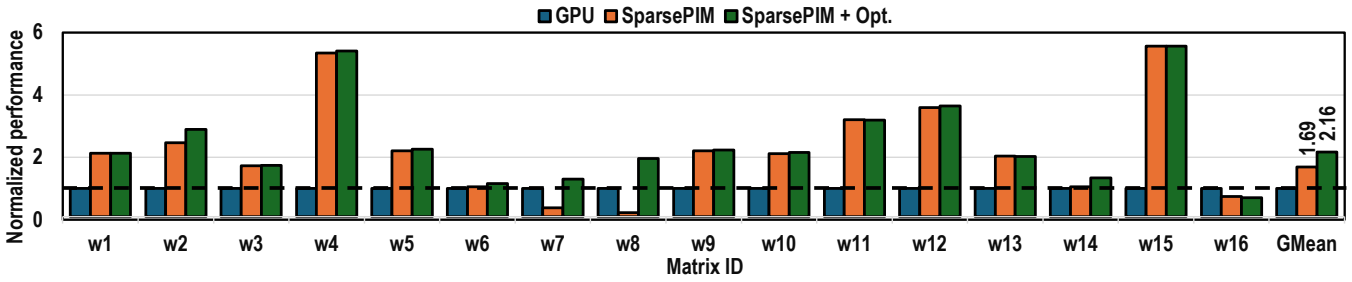


Figure 8: Performance

6.3 Performance

Figure 8 presents the performance evaluation results in terms of execution time, normalized to the baseline performance of the GPU using cuSPARSE. The results indicate that standard deviation, Jaccard similarity score, and DRAF-related overhead jointly influence the observed performance. SparsePIM without software optimization (SparsePIM + Opt.) achieves a geometric mean speedup of 1.69× over the GPU baseline, and this increases to 2.16× when software optimization is applied. The maximum speedup observed is 5.61× when both SparsePIM and software optimization are used. However, performance degrades slightly in the case of workload w16.

For workloads such as w6, w7, w14, and w16, which exhibit a fraction of non-zero elements smaller than 10^{-5}, the performance gain compared to the GPU is relatively limited. This is because the computational cost associated with zero-padding in DRAF, illustrated in Figure 11, becomes less dominant as the number of non-zero elements increases. In particular, workload w16 shows improved standard deviation, as seen in Figure 10, and improved Jaccard similarity score, shown in Figure 9. However, performance degradation is observed regardless of software optimization. This is attributed to the relatively high overhead of converting the compressed format to DRAF, which increases both memory usage and the number of operations due to the characteristics of SparsePIM. Since SparsePIM performs synchronous column access across all banks, an increase in padded zero elements directly translates to increased computational load and memory latency.

An analysis of the sparse matrix structure shows that, except for workloads w1, w6, w7, w9, w14, and w16, all other workloads contain more than one non-zero element per column. Among these, w6 has 30.05% of its columns with only one non-zero element, while in w1, w7, w9, and w14, approximately 3.75% of columns contain a single non-zero element. In contrast, w16 exhibits an extreme case in which 91.94% of the columns contain only one non-zero element. This structure significantly increases the number of padded zeros required to align the number of values per group to 16 in DRAF, thereby causing substantial overhead in both memory and computation.

In the case of w7 and w8, the application of software optimization results in a notable performance improvement compared to their unoptimized performance. This improvement arises because software optimization significantly reduces memory usage when converting the matrix to DRAF, in contrast to the conventional tiling-based approach. Since the amount of zero padding in DRAF depends on the placement of matrix columns, the memory footprint and access time are reduced when column placement is optimized.

For other workloads, SparsePIM outperforms the GPU baseline, but the additional performance gains from software optimization are negligible or even negative. This is mainly due to increased latency when the number of rows in a cluster is not divisible by four, requiring all bank groups to wait until the remaining rows are processed. In such cases, the benefits of optimization diminish. Moreover, for workloads where DRAF memory usage is already low or lower than that of COO, the added benefit of software optimization is minimal. Ultimately, SparsePIM performance is highly sensitive to the number of non-zero elements and the extent of zero padding, as these factors significantly affect both the number of memory accesses and the time required to retrieve partial results.

6.4 Evaluation of software optimization

6.4.1 *Row Index Similarity.*

In this section, we describe the effects of applying the software optimization methodology introduced in Section 5.1 to input matrix clustering. To evaluate the performance improvement, we use as our baseline a naive clustering method that partitions the original sparse matrix into K clusters by dividing the column vectors sequentially such that each cluster contains an equal number of columns. This baseline approach resembles the 1D-partitioning scheme proposed in [15].

Due to the architectural characteristics of SparsePIM, higher row index similarity among the non-zero elements processed within each BG accumulator leads to improved parallelism and, consequently, enhanced computational efficiency. To verify this effect, we evaluated the row index similarity of columns within each cluster using a score based

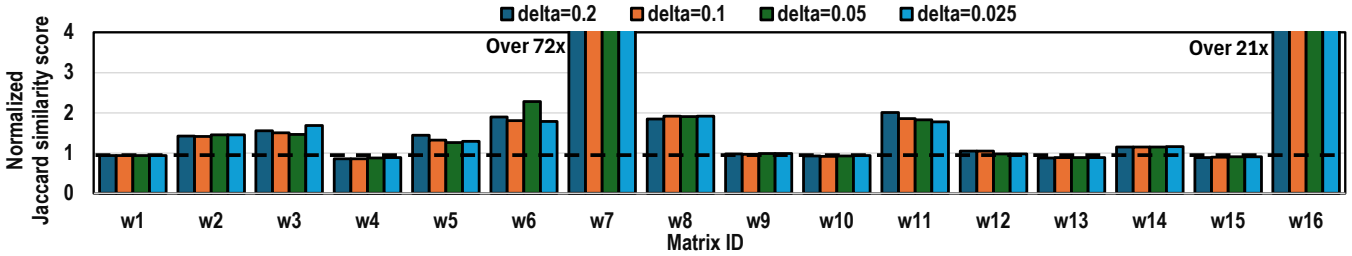


Figure 9: Jaccard similarity

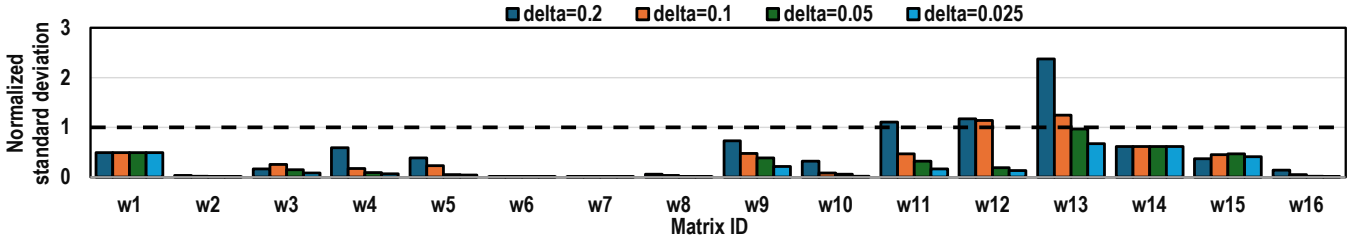


Figure 10: Standard deviation

on Jaccard similarity. The Jaccard similarity between two columns A and B is defined as $J(A,B) = \frac{|A \cap B|}{|A \cup B|}$, where A and B represent the sets of row indices containing non-zero elements in each column within the same cluster. To assess overall similarity within a cluster, the Jaccard similarity is computed for all possible pairs of columns, and the average of these values is used. This per-cluster average is then further averaged across all clusters to obtain a final Jaccard similarity score.

Figure 9 shows the Jaccard similarity score after applying software optimization, normalized to the unoptimized baseline. Based on preliminary experiments, the hyperparameters *maxIter*, *refineIter*, and *threshold* were heuristically set to 30, 5, and 0.2, respectively. We varied the *delta* parameter, which is an essential hyperparameter controlling load imbalance, and visualized its impact on the Jaccard similarity score.

Experimental results show that, across nearly all workloads and *delta* values, row index similarity significantly improves compared to the baseline. In particular, workloads w7 and w16 exhibit up to 72× and 21× increases, respectively, in Jaccard similarity score across all *delta* values. These results indicate that the clustering methodology effectively groups columns with highly overlapping row indices. Consequently, when each cluster is mapped to a BG and accumulation is performed using the BGA, the throughput of accumulation operations can be substantially improved.

6.4.2 Load Imbalance.

Our software optimization methodology reduces the imbalance in the number of non-zero elements across clusters by first applying *bounded cap K-means* and then refining the distribution through an additional *Refinement* phase. We

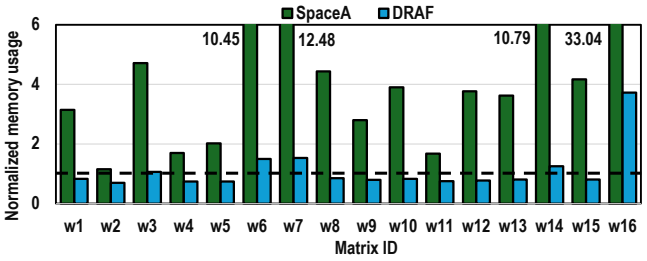


Figure 11: Memory usage of COO, SpaceA's method, and DRAF

use the standard deviation of the number of non-zero elements across clusters as the evaluation metric to quantify the effectiveness of this approach. A lower standard deviation indicates that the clusters' number of non-zero elements is closer to the mean, signifying a more uniform data distribution. Figure 10 illustrates the results normalized against the baseline for the case where *Refinement* is applied. Across all of the sparse suite workload inputs, the software optimization shows a normalized standard deviation of less than 1 when hyperparameter *delta* is smaller than 0.05, indicating that each cluster's number of non-zero elements is more evenly distributed compared to the baseline. As the number of non-zero element balanced clusters is fed into the BGAs for accumulation, the runtime discrepancy among accumulators diminishes, enhancing resource utilization and reducing idle time overall.

6.5 Evaluation of DRAF

Figure 11 compares the memory usage of the proposed DRAF format with the conventional COO format and the mapping

method previously proposed by SpaceA [88]. The sparse suites are arranged in the same order as Table 3. For DRAF, we include the memory space used for storing vectors and sparse matrices, including the empty area, while excluding only the space reserved for partial result storage. In most cases, except for w3, w6, w7, w14, and w16, DRAF reduces memory usage by an average of 21.28% compared to COO, with the most significant reduction observed in w2, where memory usage decreases by up to 29.82%. However, in the case of w16, DRAF increases memory usage by up to 3.7× compared to COO. This overhead occurs when many columns contain fewer than 16 non-zero values or when the number of values per column is not divisible by 16. Nonetheless, since DRAF aligns data according to the access granularity required for computation, it can tolerate such overhead in a limited number of cases.

In contrast, the mapping method proposed by SpaceA stores matrix values by mapping each DRAM row to one matrix row, and under the configuration assumed in this work (1KB row buffer, 2B data, and 4B for each row and column index), this approach can waste up to 1,014 bytes of space per row. In the worst case, only a single data element can reside in a DRAM row, resulting in severe inefficiency. As a result, SpaceA's mapping method increases memory usage by between 1.2× and 33.0× compared to COO. In particular, w6, w7, w14, and w16 exhibit more than 10× overhead, which correlates with their high fraction of non-zero elements. In contrast, DRAF achieves significantly better efficiency and reduces overhead by a geometric mean of 4.34× compared to SpaceA, demonstrating its practicality and suitability for DRAM-based sparse matrix storage.

6.6 Power and area

We measured the power consumption and area of the BGA using Synopsys Design Compiler. Specifically, we evaluated the area of the newly added components, such as the index queue pair, comparator, register read/write unit, adder controller, and flush controller, while excluding the SIMD FPU from the measurement. The result shows that the BGA consumes 31.85 μW of dynamic power. For comparison, we designed a 16-lane SIMD multiplier identical to the one embedded in HBM-PIM, using the same 14nm process. The measurement result shows that the SIMD multiplier consumes 34.51 μW, which is 8% higher than the BGA. Based on these results and existing HBM-PIM power data, we conclude that SparsePIM can operate without exceeding the thermal design power (TDP) limit of HBM2.

For the area comparison, we used a 14nm process for the BGA, in contrast to the different technology node used in HBM-PIM. Therefore, instead of comparing physical cell area, we compared gate counts with the HBM-PIM design. In SparsePIM, a bank group consisting of four banks shares one processing unit, whereas HBM-PIM assigns one processing unit to every two banks. As a result, the BGA increases the gate count by only 2.2% compared to the original HBM-PIM processing unit. In contrast, pSyncPIM [5] increases the area by 35.8% over HBM-PIM. SparsePIM achieves SpMV acceleration while occupying less area and staying within thermal constraints, demonstrating both area and power efficiency.

7 Conclusion

In this paper, we propose SparsePIM, an HBM-based PIM architecture for accelerating SpMV kernels. SparsePIM includes a software optimization approach, a new sparse matrix compression format, and an efficient processing in-memory architecture to perform SpMV operations. By applying the proposed software optimization, SparsePIM improves the parallel computations by increasing the row index similarity within a column group to solve the load imbalance issues. In addition, we propose a new compressed format, called DRAF, to facilitate operations according to data access granularity. In the case of the proposed SparsePIM, we enable SpMV, a sparse operation, in existing PIMs that only support dense BLAS operations, such as existing matrix-vector or vector-scalar multiplication, through the BGA. The standard deviation results show that the load imbalance problem is improved through SW optimization, and the Jaccard similarity scores show that the row index similarity is increased for most workloads, which increases parallelism when accumulating partial results. According to the experimental results, the performance was improved by an average of 2.16× and up to 5.61× speedup compared to the cuSPARSE-based GPU. In addition, the TDP and logic area met the requirements of HBM2 despite efficiently processing SpMV operations. Our approach lays a foundation for future PIM architectures capable of efficiently handling irregular data patterns.

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